Encoder phase terminals > PORTA bits 0 - 7
- generate interrupts
Encoder quad terminals > PORTC bits 2 - 7 and PORTF bits 6 and 7
- read by ISR to determine if up or down
(These signals are lost on reaching the next click stop
- but the ISR is fast !)
NB: PORTC bits 0 and 1 are shared by the I2C interface
and so cannot be used for the quad inputs of encoders 0 and 1)

RS232 connector
- this is configured as if it were a PC.
eg: FTDX101 specifies s 'straight'
cable (no crossover) because it receives
on pin 3 and transmits on pin 2.
(See FTDX101 AF-unit circuit diagram
... which also uses the ADM3202
RS232 interface device)

The PCA9600 is a dual open drain bidirectional bufffer
supporting voltage level change, and up to 15v pullup.
It is intended for I2C transmission via CAT cable.
(SCL and SDA are each spilt into CAT pairs, one in each direcrtion.
- It has high current capability so 100R termination is feasible on 5v)
We use it in reverse here.
Its advantage for CI-V is that the buffer output on pin 1
pulls down to 0.5v which is above the 'low' threshold for the input.
Therefore, the transmitted bytes are not reflected back
to the USART.

G3VPX - ENCAT (issue 3) schematic
(Rotary encoder to rig interface)
24th January 2020

Issue3 - Icom CI-V support added